

WHAT IS CLAIMED IS:

1. A method for accessing initialization data for starting a central processor unit in a computer system comprising:
starting up a north-bridge chip;
5 requesting said initialization data by said north bridge chip from a south bridge chip;
receiving said initialization data by said north-bridge chip .
2. The method according to Claim 1 wherein said initialization data is serial initialization packet ("SIP") [?] data of the central processor unit.
- 10 3. The method according to Claim 2 wherein said initialization data is SIP data of AMD K7 processor.
4. The method according to Claim 1 wherein the starting up a north-bridge chip further includes starting up the north-bridge chip by said south-bridge chip.
5. The method according to Claim 1 wherein the requesting further includes
15 sending a signal from said north bridge chip to said south-bridge chip for requesting said initialization data.
6. The method according to Claim 1 further comprising sending said initialization data to the central processor unit of said computer system for starting up the central processor unit.
- 20 7. A method for accessing initialization data of a central processor unit by a south-bridge chip in a computer system comprising:
accessing said initialization data by said south-bridge chip; and
sending said initialization data by said south-bridge chip.

8. The method according to Claim 7 wherein said initialization data is SIP data of AMD K7 processor.

9. The method according to Claim 7 wherein said south-bridge chip accesses said initialization data from boot ROM of said computer system.

5 10. The method according to Claim 7 wherein said south-bridge chip accesses said initialization data after a north-bridge chip of said computer system is started up by said south-bridge chip and sends a signal to request said initialization data.

10 11. The method according to Claim 10 wherein said north-bridge chip sends said initialization data to a central processor unit of said computer system.

12. A method for accessing initialization data for starting a central processor unit in a computer system, the method comprising:

requesting the initialization data by a north bridge chip from a south bridge chip;

15 accessing the initialization data stored in a non-volatile memory by the south bridge chip; and

activating the central processor unit based on the initialization data received by the north-bridge chip from the south bridge chip.

20 13. The method of claim 12 further comprising activating the north bridge chip by sending an initiating signal from the south bridge chip.

14. The method of claim 12 further comprising activating the south bridge chip by a power supplier.

15. The method of claim 12 wherein the non-volatile memory is a read only memory containing BIOS.

16. The method of claim 12 wherein the requesting further includes sending a transaction from the north bridge chip to the south-bridge chip requesting the south bridge chip to retrieve the initialization data from the non-volatile memory.

17. The method of claim 12 wherein the activating further includes:

5 receiving the initialization data by the north bridge chip; and
 sending an initializing signal and the received initialization data to the central processor unit .

18. The method of claim 17 wherein the initialization data further includes an initialization ID.

10 19. The method of claim 17 wherein the initialization data further includes serial initialization packet ("SIP") data.

20. A system for accessing initialization data for starting a central processor unit, the system comprising:

 a north bridge chip in direct communication with a south bridge chip and
15 the central processor unit; and

 a non-volatile memory subsystem in direct communication with the south bridge chip storing the initialization data;

 wherein upon receiving a request from the north bridge chip for obtaining the initialization data, the initialization data is accessed by the south bridge chip
20 and forwarded to the north bridge chip for activating the central processor unit.

21. The system of claim 20 further comprising a power supplier for activating the south bridge chip.

22. The system of claim 20 wherein the non-volatile memory is a read only memory containing BIOS.

23. The system of claim 22 wherein the non-volatile memory includes a predetermined location for storing the initialization data that is not occupied by the BIOS.

24. The system of claim 20 wherein the initialization data further includes an initialization ID.

25. The system of claim 20 wherein the initialization data further includes session initialization protocol data.

26. The system of claim 20 wherein the south bridge chip further includes means for:

activating the north bridge chip;
retrieving the initialization data by the south bridge chip; and
sending the initialization data to the north bridge chip.

27. The system of claim 20 where in the north bridge chip further includes means for sending an initializing signal to the central processor unit based on the forwarded initialization data.

28. A method for accessing initialization data for starting a central processor unit in a computer system, the method comprising:

activating a south bridge chip by a power supplier controller;
activating a north bridge chip by the activated south bridge chip;
requesting the south bridge chip to access the initialization data;
accessing the initialization data stored in a non-volatile memory by the south bridge chip;
sending the initialization data to the north bridge chip by the south bridge chip;

sending an initialization signal to the central processor unit by the north bridge chip upon receiving the initialization data; and

activating the central processor unit by the initialization signal.

29. The method of claim 28 wherein the non-volatile memory is a read only
5 memory containing BIOS.

30. The method of claim 28 wherein the initialization data further includes an initialization ID.

31. The method of claim 28 wherein the initialization data further includes session initialization protocol data.

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